What is claimed is:

1. A ferroelectric memory device, comprising:

a semiconductor substrate structure having a transistor;

a lower electrode formed on an interfacial insulation layer and connected to a source/drain region of the transistor through a contact by passing through the interfacial insulation layer;

an isolating insulation layer on the interfacial insulation layer, the isolation insulation layer having a planarized surface exposing a surface of the lower electrode and encompassing the lower electrode;

a ferroelectric layer covering the isolating insulation layer and lower electrode;

an oxygen vacancy compensation layer being formed on the ferroelectric layer and compensating an oxygen vacancy caused by deoxidization of a composition of the ferroelectric layer; and

an upper electrode formed on the oxygen vacancy compensation layer.

2. The ferroelectric memory device as recited in claim 1, wherein a metal oxide layer is used to form the oxygen vacancy compensation layer.

3. The ferroelectric memory device as recited in

claim 2, wherein a ruthenium oxide layer or iridium oxide layer is used to form the metal oxide layer.

4. The ferroelectric memory device as recited in claim 1, wherein the oxygen vacancy compensation layer has a thickness ranging from about 10 Å to about 1000 Å.

5. The ferroelectric memory device as recited in claim 1, wherein, one of materials as a high density plasma (HDP) oxide layer, boro phospho silicate glass (BPSG), Boro phospho silicate BSG and phosphor PSG is used to form the isolating insulation layer.

6. The ferroelectric memory device as recited in claim 1, wherein the lower electrode sequentially includes a glue layer, an oxide barrier layer and a metal layer.

7. The ferroelectric memory device as recited in claim 6, wherein an iridium layer, an iridium oxide layer, and a platinum layer are used to form the glue layer, the oxygen layer, the metal layer, respectively.

8. A method for fabricating a ferroelectric memory device, comprising the steps of:

a) forming an interfacial insulation layer on a semiconductor substrate;

b) forming a stack pattern of a lower electrode and a

hard mask on the interfacial insulation layer;

c) forming an isolating insulation layer on an entire surface having the stack pattern;

d) planarizing an isolating insulation layer until exposing a surface of the hard mask;

e) removing the hard mask by using a liquid chemical;

f) forming a ferroelectric layer on an entire surface having the lower electrode exposed after the hard mask is removed;

g) forming an oxygen vacancy compensation layer on the ferroelectric layer;

h) forming a conductive layer for an upper electrode on the oxygen vacancy compensation layer; and

i) patterning the conductive layer and the oxygen vacancy compensation layer consecutively.

9. The method as recited claim 8, wherein one of materials as $SrBi_2(Ta_{1-x}, Nb_x)_2O_9$ (SBTN), $SrBi_2Ta_2O_9$ (SBT), $Bi_4Ti_3O_{12}$ (BTO), and $Bi_{4-x}La_xTi_3O_{12}$ (BLT) is used in order to form the ferroelectric layer.

10. The method as recited in claim 8, wherein the oxygen vacancy compensation layer is a metal oxide layer deposited at a temperature of about 100 ℃ to about 700 ℃ and at a pressure of about 0.1 mtorr to about 10 torr by employing a chemical vapor deposition (CVD) or an atomic layer deposition (ALD) technique.

11. The method as recited in claim 10, wherein the metal oxide layer is a ruthenium oxide layer or iridium layer.

12. The method as recited in claim 8, wherein the oxygen vacancy compensation layer has a thickness ranging about 10 Å to about 1000 Å.

13. The method as recited in claim 8, wherein the isolating insulation layer is planarized until exposing the surface of the hard mask by performing a chemical mechanical polishing (CMP) process.

14. The method as recited in claim 8, wherein one of materials as a HDP oxide layer, BPSG, BSG and PSG is used to form the isolating insulation layer.